IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

1. (Currently Amended) A method of chained switching execution of data processing tasks, comprising:

a first data processing task executing a call to a task switching function;

the task switching function selecting a return address corresponding to a second data processing task different from the first data processing task;

the task switching function executing a return operation to the second data processing task;

the second data processing task executing a call to the task switching function;

the task switching function selecting a return address corresponding to a third data processing task different from the first and the second data processing tasks; and

the task switching function executing a return operation to the third data processing task.

2. (Original) The method of Claim 1, wherein said selecting step includes the task switching function selecting a first pointer that points to a first area of memory where said return address is stored.

3. (Original) The method of Claim 2, wherein said pointer selecting step includes updating a second pointer to point to said first pointer.

4. (Original) The method of Claim 3, wherein said updating step includes updating the second pointer from a status wherein the second pointer points to a third pointer to a status

wherein the second pointer points to said first pointer, and wherein said third pointer points to a second area of memory.

5. (Original) The method of Claim 4, wherein a return address corresponding to said first data processing task is stored in said second area of memory.

6. (Original) The method of Claim 5, including the task switching function storing said third pointer.

7. (Original) The method of Claim 1, including the task switching function deselecting a return address corresponding to the first data processing task.

8. (Original) The method of Claim 1, including saving a return address corresponding to the first data processing task, and executing said saving step in parallel with said call executing step.

9. (Original) The method of Claim 1, wherein said first data processing task is one of a host task, a disk task and a servo task of an optical drive control system, and wherein the second data processing task is another of said host task, said disk task and said servo task.

10. (cancelled)

11. (Previously Presented) An apparatus for chained switching execution of tasks on a data processor, comprising:

a memory having a first storage location for storing a return address corresponding to a second task;

an input for receiving information indicative of instructions of a task switching function that has been called by a first task;

a memory management apparatus coupled to said input and said memory, and responsive to said instruction information indicating a return instruction for moving said return address from said first storage location to a register of the data processor;

the memory having a second storage location for storing a return address corresponding to a third task;

the input receiving information indicative of instructions of a task switching function that has been called by the second task; and

the memory management apparatus responsive to said instruction information indicating a return instruction for moving said return address corresponding to said third task from said second storage location to a register of the data processor.

12. (Original) The apparatus of Claim 11, wherein said memory includes a second storage location for storing a first pointer which points to a first area of said memory that includes

said first storage location, said memory management apparatus responsive to said instruction information for selecting said first pointer.

13. (Original) The apparatus of Claim 12, wherein said memory management apparatus includes a memory manager for maintaining a second pointer, said memory manager responsive to said instruction information for updating said second pointer to point to said first pointer in said memory.

14. (Original) The apparatus of Claim 13, wherein said memory manager is operable for updating said second pointer from a status wherein said second pointer points to a third pointer stored at a third location in said memory to a status wherein said second pointer points to said first pointer, and wherein said third pointer points to a second area of said memory.

15. (Original) The apparatus of Claim 14, wherein said second area of said memory includes a fourth storage location which stores therein a return address corresponding to said first data processing task.

16. (Original) The apparatus of Claim 15, wherein said memory manager is responsive to said instruction information for storing said third pointer in said third location of said memory.

17. (Previously Presented) A data processing apparatus, comprising:

a data processing portion for executing data processing tasks;

a task switcher coupled to said data processing portion for switching from execution of a first task to execution of a second task, said task switcher including a memory having a storage location for storing a return address corresponding to the second task, and an input for receiving information indicative of instructions of a task switching function that has been called by the first task;

a register coupled to said task switcher; and

said task switcher including a memory management apparatus coupled to said input and said memory, and responsive to said instruction information indicating a return instruction for moving said return address from said storage location to said register;

the task switcher switching from execution of the second task to execution of a third task, said memory having a storage location for storing a return address corresponding to the third task, and an input for receiving information indicative of instructions of a task switching function

that has been called by the second task.

18. (Original) The apparatus of Claim 17, wherein said task switcher includes a portion of a TriCore data processor architecture.

19. (Original) The apparatus of Claim 17, wherein said register is a program counter register.

20. (Original) The apparatus of Claim 17, wherein said first data processing task is one of a host task, a disk task and a servo task of an optical drive control system, and wherein the second data processing task is another of said host task, said disk task and said servo task.